Electronic Version
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Claims

[c1] A method of enhancing stress in a semiconductor device having a gate stack disposed on a substrate, comprising: depositing a nitride film along a surface of the substrate and the gate stack, wherein the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack.

[c2] The method of claim 1, further comprising forming a spacer adjacent only a lower portion of the gate stack.

[c3] The method of claim 2, wherein forming the spacer comprises reducing a size of the spacer.

[c4] The method of claim 3, wherein reducing the spacer comprises reactive ion etching.

[c5] The method of claim 1, wherein the nitride film is a non-conformal nitride film.

[c6] The method of claim 1, wherein depositing the nitride film comprises a plasma enhanced vapor deposition process.

[c7] The method of claim 1, wherein the deposition of the nitride film provides enhanced stress within a transistor

channel.

[c8] A method of enhancing stress in a semiconductor device, comprising:
depositing a layer of nitride film over a gate stack and a surface of a substrate; and
removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack.

[c9] The method of claim 8, further comprising depositing a resist material on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack exposed.

[c10] The method of claim 9, further comprising removing an upper portion of the gate stack and the nitride film disposed thereon.

[c11] The method of claim 9, wherein depositing the resist comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material.

[c12] The method of claim 11, further comprising forming spacers at a lower portion of the sidewalls of the gate stack.

[c13] The method of claim 11, wherein forming the spacers

includes forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls.

[c14] The method of claim 11, wherein depositing a resist comprises depositing at least one of an oxide layer or a borophosphorosilicate glass on low spots and leaving high spots exposed.

[c15] The method of claim 10, wherein removing a portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching.

[c16] The method of claim 10, wherein removing a portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing.

[c17] The method of claim 8, further comprising forming a spacer adjacent a sidewall of the gate stack and etching upper portions of the spacer to form sidewalls only at a lower portion of the sidewalls.

[c18] The method of claim 8, wherein the gate is about 60 nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 4.5×10^9 dynes/cm^2 at about 5 nm below a gate oxide.

[c19] The method of claim 8, wherein for a semiconductor device having a gate about 60 nm wide, a spacer about 50 nm wide, and a nitride film stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately 5.5 x 10^9 dynes/cm^2 at about 5 nm below a gate oxide.

[c20] A semiconductor device, comprising:
a silicon substrate;
a gate stack disposed on the silicon substrate;
a stressed nitride film on the silicon substrate and the gate stack, wherein the stressed nitride film is thicker over the silicon substrate and thinner over a portion of the gate stack.

[c21] The semiconductor device of claim 20, wherein the stressed nitride film is substantially absent the upper portion of the gate stack.

[c22] The semiconductor device of claim 20, further comprising spacers disposed on the substrate between the stressed nitride film and the gate stack leaving an upper portion of the gate stack exposed.

[c23] The semiconductor device of claim 21, further comprising only a lower portion of the gate stack.

[c24] The semiconductor device of claim 23, further compris-

ing a spin-on material disposed over the stressed nitride film leaving the gate stack exposed.